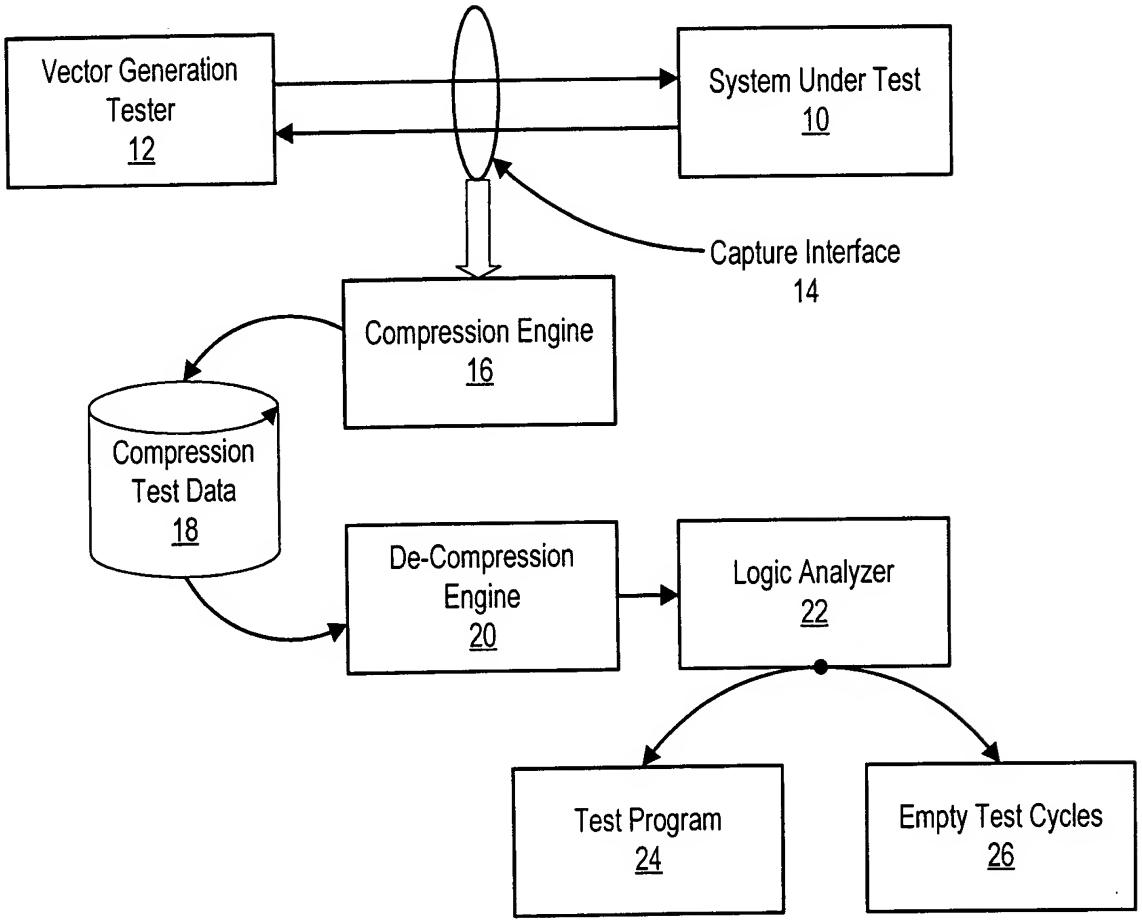
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System Under Test
10
Capture Interface
14
Compression Engine
16
Compression
Test Data
18
De-Compression
Engine
20
Logic Analyzer
22
Test Program
24
Empty Test Cycles
26

Figure 1

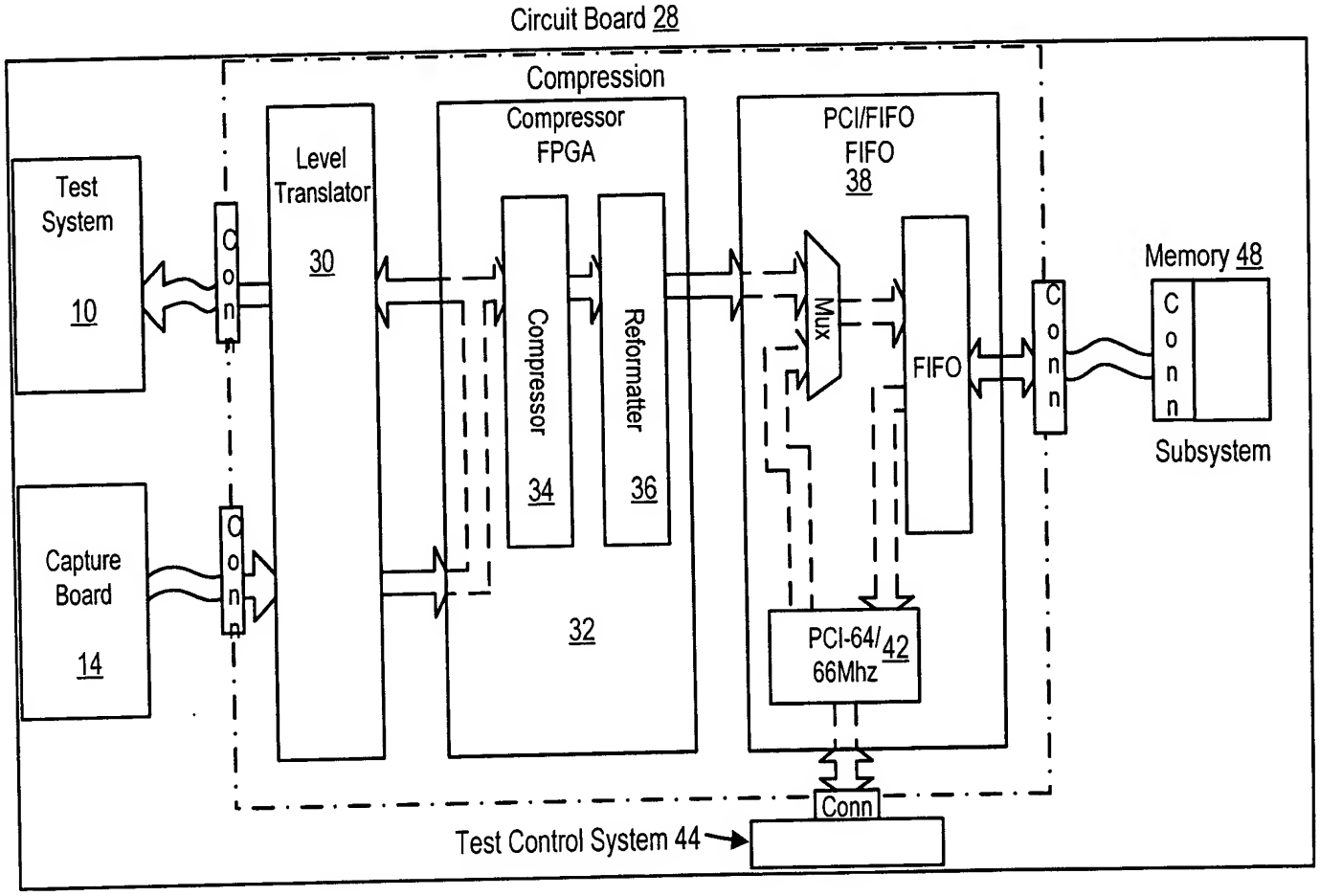
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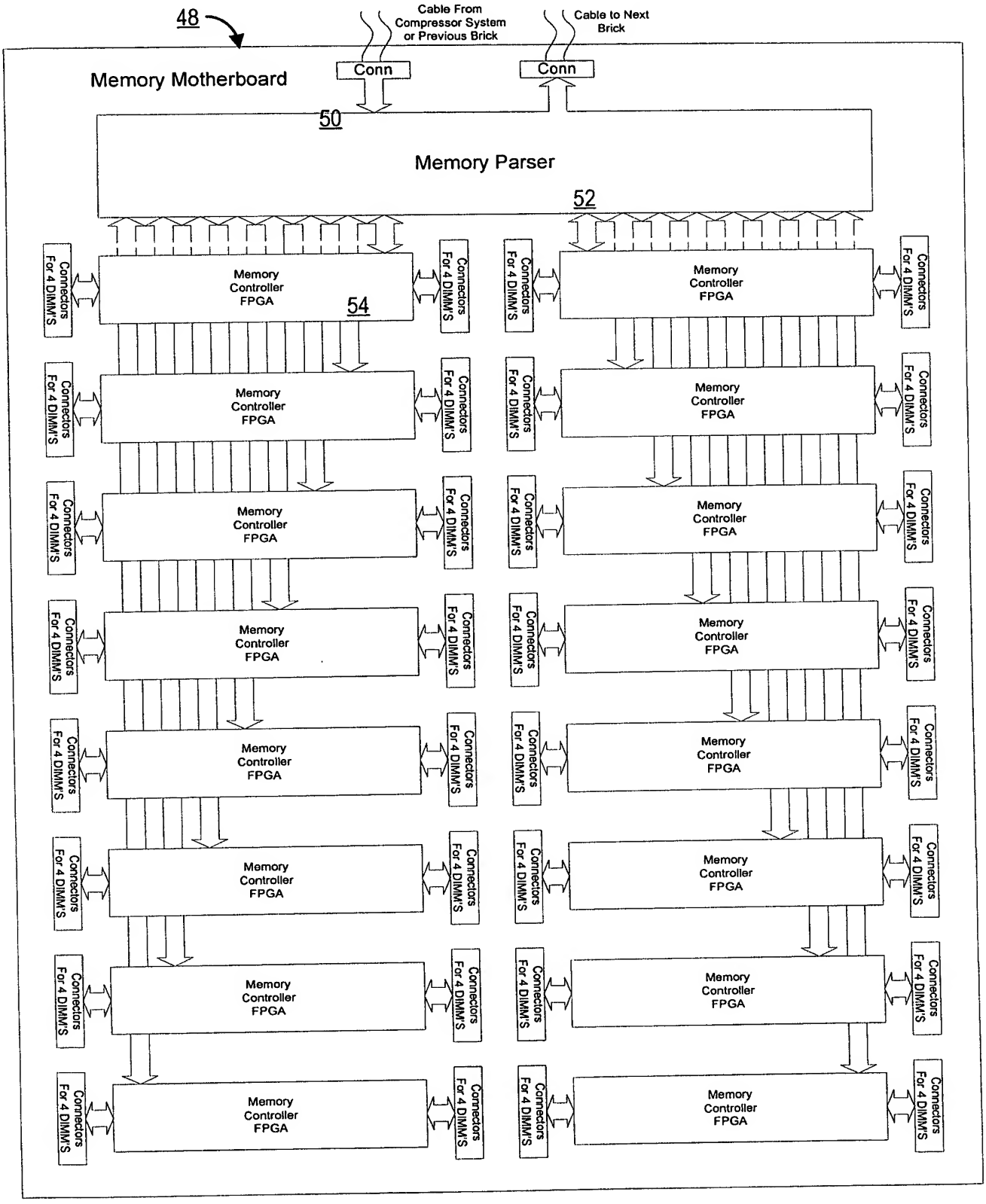
Figure 2


48
Cable From Compressor System or Previous Brick
Cable to Next Brick
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Conn
Memory Motherboard
50
Memory Parser
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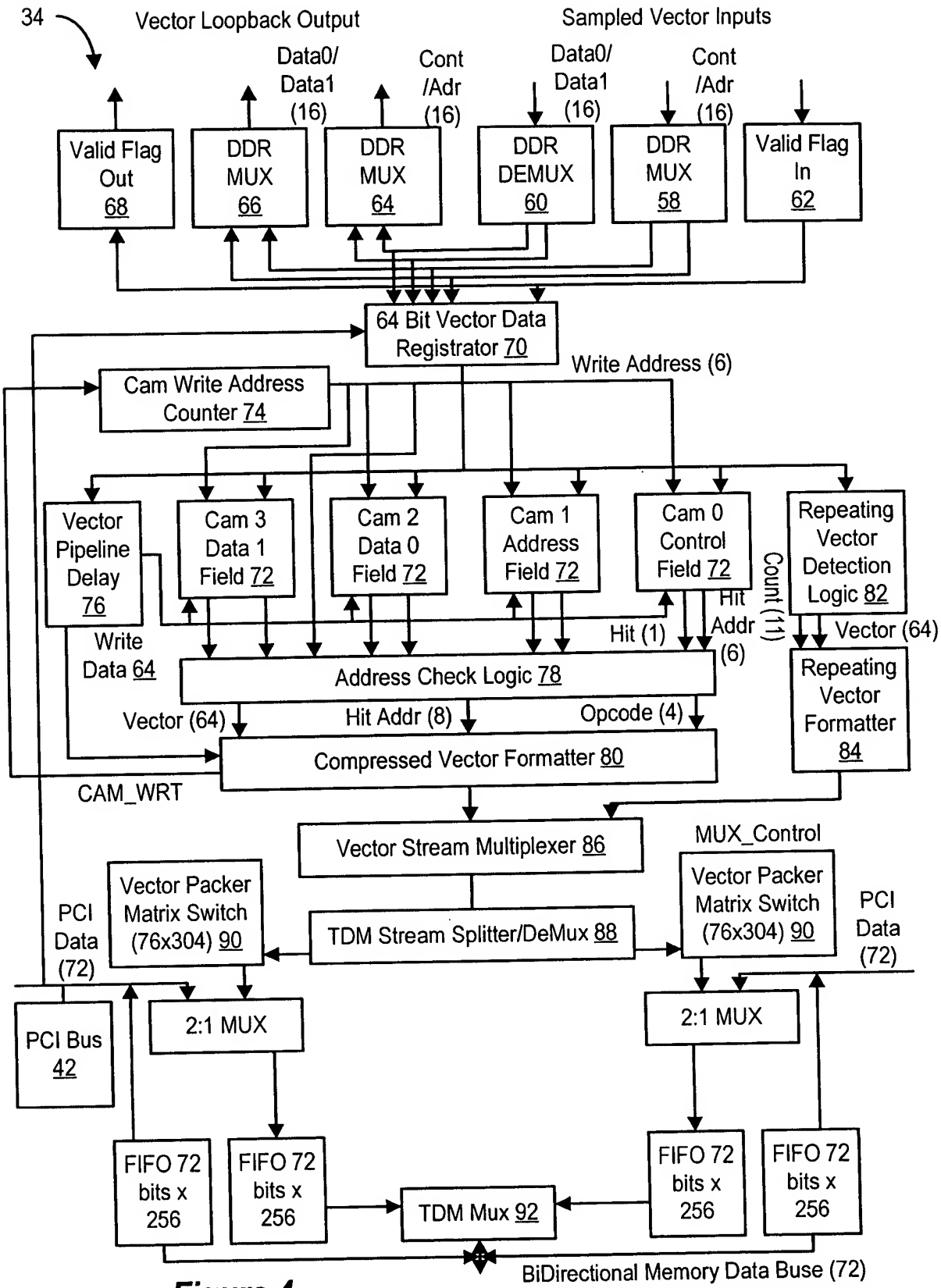
Memory Controller FPGA
54
Connectors For 4 DIMM'S

Figure 3


34
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Data0/ Data1 (16)
Cont /Adr (16)
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2:1 MUX
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FIFO 72 bits x 256
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FIFO 72 bits x 256
FIFO 72 bits x 256
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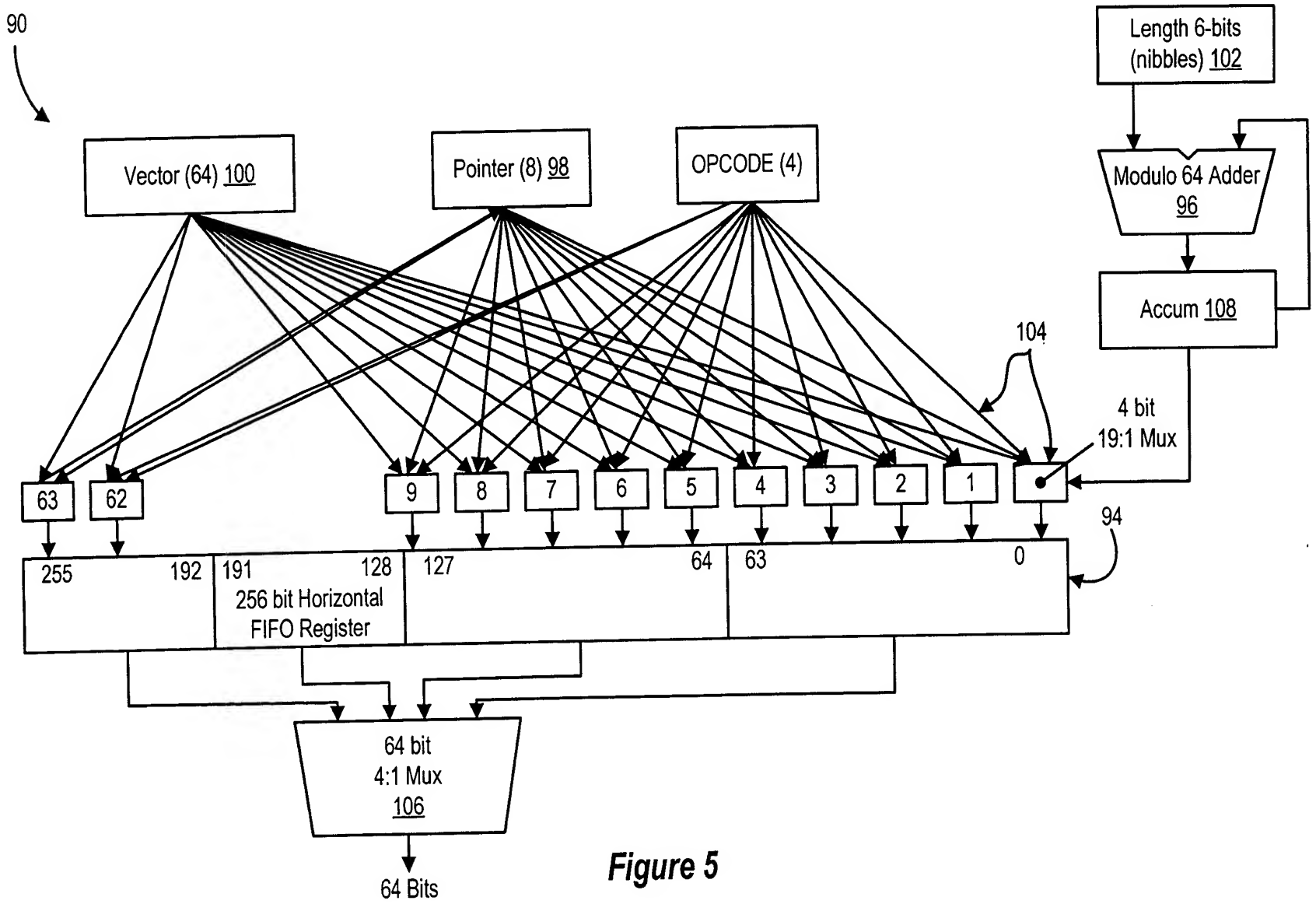
Figure 4


90
Length 6-bits
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104
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9
8
7
6
5
4
3
2
1
94
255
192
191
128
127
64
63
0
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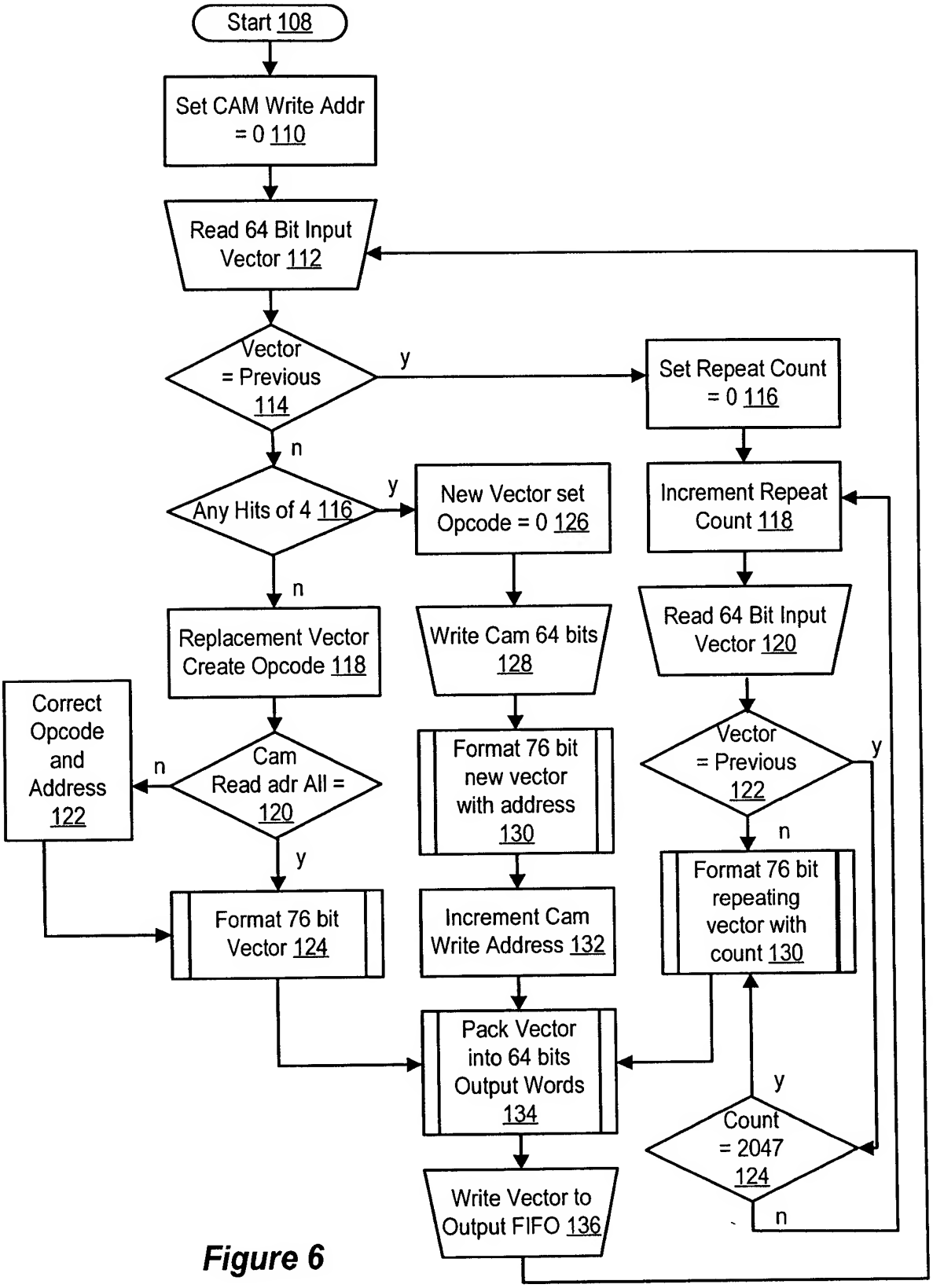
FIFO Register
64 bit
4:1 Mux
106
64 Bits

Figure 5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Set CAM Write Addr = 0 110
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y
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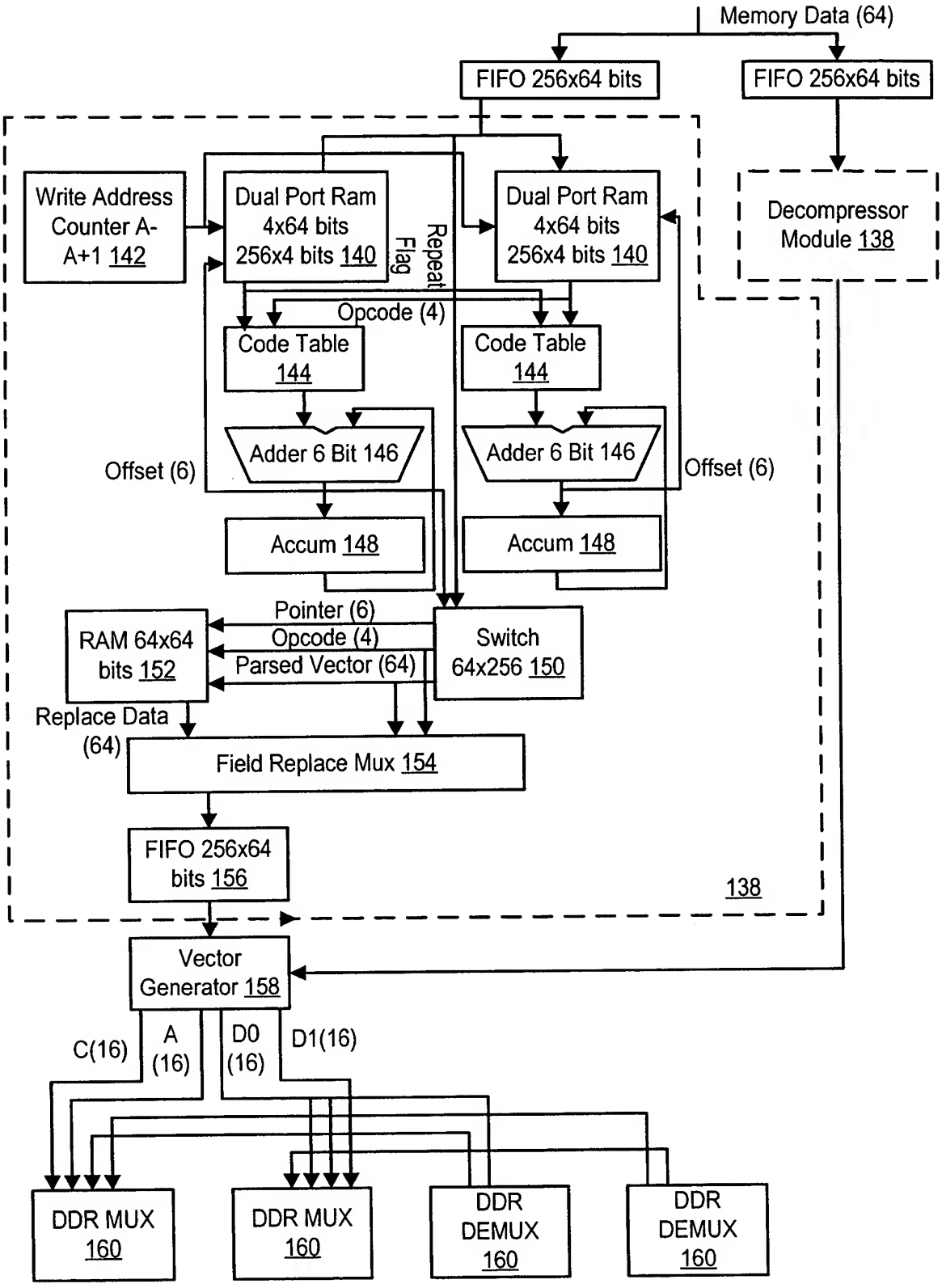
Figure 6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DDR MUX 160
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DDR DEMUX 160

Figure 7